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10/616,802	07/10/2003	Barinder Singh Rai	VP070	2294

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EPSON RESEARCH AND DEVELOPMENT INC
INTELLECTUAL PROPERTY DEPT
150 RIVER OAKS PARKWAY, SUITE 225
SAN JOSE, CA 95134

EXAMINER	
FLOURNOY, HORACE L	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,802	RAI ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 1/10/2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/10/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 10 January 2006. Claims 1-26 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments. Furthermore, new grounds for rejection have been set forth as a result of the instant amendments. Accordingly, this action has been made FINAL, as necessitated by amendment.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statement dated **07/10/2003** is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-16, 18-21, and 23-24, are rejected under 35 U.S.C. 103(a) as being obvious over Blodgett (U.S. Patent no. 6,401,186 hereafter referred to as Blodgett) in view of - Laurenti et al. (US Patent No. US 6,658,578 hereafter referred to as Laurenti).

With respect to the limitation of **independent claims 1, 6, 11, 16, and 21,**

"A method for optimizing memory bandwidth, comprising: requesting data associated with a first address; 'obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor; **[Blodgett discloses in column 6, lines 62-67, "The column address generated in the absence of a request by**

the microprocessor can be determined in any number of ways."] *storing the data associated with the first address and data associated with the consecutive address in a temporary data storage area;* **[Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2."]** *requesting data associated with a second address;* **[Blodgett discloses this limitation, e.g. in column 6, lines 21-29]** *and determining whether the data associated with the second address is stored in the temporary data storage area ~~through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address."* **[See Fig. 153 of Laurenti and associated text]**

Blodgett does not expressly teach the limitations cited supra by Laurenti.

Blodgett and Laurenti are analogous art because they are from the same field of endeavor, that being data pre-fetching.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the method of claim 1 in which data is requested, obtained, and stored in for an associated address with a determining factor based on most or least significant bits to arrive at independent **claims 1, 6, 11, 16, and 21.** Furthermore, after data is prefetched it is accessed like any other data.

The motivation for doing so would have been obvious based on the teaching of Laurenti in column 161, lines 25-40 and column 163 lines 50-column 164, line 5.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Blodgett and Laurenti before him/her to combine Laurenti and Blodgett for the benefit of having a system that can data is requested, obtained, and stored in for an associated address with a determining factor based on most or least significant bits to obtain the invention as specified in **claims 1, 6, 11, 16, and 21**.

With respect to **claim 2**,

"The method of claim 1, wherein the method operation of obtaining the data associated with the first address and data associated with a consecutive address from a memory region in a manner transparent to a microprocessor includes, completing the obtaining the data associated with the first address and data associated with a consecutive address in one clock cycle associated with the microprocessor." **[is disclosed in column 3, lines 15-18 and FIGs. 1, 3, 4, 6, and 7]**

Blodgett discloses in column 3, lines 15-18, "In a burst read cycle, data within the memory located at the row and column address selected by the row and column address decoders is read out of the memory and sent along data path 32 to output latches 34."

Blodgett teaches completing the obtaining the data (read out of the memory) associated with the first address and data associated with a consecutive address (memory located at the row and column address selected) in one clock cycle associated with the microprocessor (See FIGs. 1, 3, 4, 6, and 7).

With respect to **claim 3**,

"The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the temporary data storage area ~~buffer through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal, the most significant bits being all bits except first and second least significant bits; and if the most significant bits of the signal are equal to the corresponding most significant bits of the previous signal, then the method includes, accessing the data in the temporary data storage area according to the first and second least significant bits." **[is disclosed in column 6, lines 1-28 and column 4, lines 1-17 of Blodgett]**

The examiner interprets claim 3 to as a "hit" in temporary data storage or cache and therefore does not require a fetch for needed data in the memory region.

Blodgett discloses in column 6, lines 13-21, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller. If the

addresses are the same, the memory controller continues with the new burst read operation. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor."

Blodgett teaches that via the use of a comparator (to determine whether the data associated with the second address is stored in the buffer through a configuration of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal) if a "hit" occurs.(if the most significant bits of the signal are equal to the corresponding most significant bits of the previous signal) then access the data in the temporary data storage area (If the addresses are the same, the memory controller continues with the new burst read operation).

With respect to **claim 4**,

"The method of claim 1, wherein the method operation of determining whether the data associated with the second address is stored in the temporary data storage area ~~buffer through a configuration~~ according to most significant bits of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal; and if the most significant bits of the signal are not equal to the corresponding most significant bits of the previous signal, then the method includes, fetching the data associated with the second address from the memory region; and fetching consecutive data associated with the second address from

the memory region." **[is disclosed in column 6, lines 1-28 and column 4, lines 1-17 of Blodgett]**

The examiner interprets claim 3 to as a "miss" in temporary data storage or cache and therefore requires a fetch for the needed data in the memory region.

Blodgett discloses in column 6, lines 13-21, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller. If the addresses are the same, the memory controller continues with the new burst read operation. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor."

Blodgett teaches that via the use of a comparator (to determine whether the data associated with the second address is stored in the buffer through a configuration of a signal requesting the data associated with the second address includes, comparing the most significant bits of the signal to corresponding most significant bits of a previous signal) if a "miss" occurs (if the most significant bits of the signal are not equal to the corresponding most significant bits of the previous signal) then fetch the consecutive data associated with the second address from the memory region. If the address requested by the microprocessor is different from that produced by the memory controller, a new read operation is initiated at the address provided by the microprocessor).

With respect to **claim 5**,

"The method of claim 4, further comprising: determining an amount of consecutive data to fetch according to a value associated with ~~the~~ first and second least significant bits of the signal." **[is disclosed in column 6, lines 62-67 – column 7, lines 1-8 of Blodgett]**

Blodgett discloses in column 6, lines 62-67 – column 7, lines 1-8, "The column address generated in the absence of a request by the microprocessor can be determined in any number of ways. The new address can be produced by repeating the prior sequence with an advanced most significant bit, as shown in Tables 1 where X represents address most significant bits (MSB's) followed by bits A1 and A0. In Table 1 an interleaved address sequence is shown for a burst length of 4. The next burst sequence start address is derived by incrementing the MSB's (X) and by repeating the initial LSB's (A1, A0). In Table 2 the next burst sequence start address is derived by incrementing the MSB's and resetting the LSB's to 0, 0. Either of these methods may be utilized for other burst length options, and for other addressing sequences."

Blodgett teaches determining an amount of consecutive data (burst length) to fetch according to a value associated with the least significant bits (LSB) of the signal.

With respect to **claim 7**,

"The method of claim 6, further comprising: if the next read command does not correspond to the data associated with the consecutive address, the method includes, storing data associated with the next read command in the buffer; and

storing data having a consecutive address to the data associated with the next read command in the buffer." **[is disclosed in column 6, lines 33-38, and FIG. 2]**

Blodgett discloses in column 6, lines 33-38, "A first column address (COLm) identified by the microprocessor 80 is provided to the memory 84. The first address is used as the starting address for the burst read operation. The internal address is advanced in either a sequential or interleaved manner as described above with reference to FIG. 2.

Blodgett teaches storing the data associated with the next read command (first address used as the starting address) in a buffer (memory 84) and storing data associated with a consecutive address relative to the first address in the buffer (The internal address is advanced in a sequential manner).

With respect to **claim 9**,

"The method of claim 6, wherein the method operation of storing data associated with a consecutive address relative to the first address in the buffer includes, issuing a read store select signal; and directing the data to a storage location of the buffer according to the read store select signal."

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal. Blodgett also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

With respect to **claim 10**,

"The method of claim 6, wherein the method operation of obtaining the data from the buffer includes, determining a location of the data in the buffer through a data select signal corresponding to the least significant bits of the next read command." **[disclosed in column 3, lines 46-47, 66-67, column 4, lines 1-3, and FIG.3 (Note: see all signals).]**

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal. Blodgett also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

With respect to **claims 12, 8, 18, and 24**,

"The memory controller of claim 11, wherein the logic for determining if a request for data associated with a next read operation is for the data associated with the

consecutive address in the temporary storage includes, a comparator configured to compare the corresponding most significant bits of a signal corresponding to the request for data associated with a next read operation with a signal corresponding to the address for the read operation." **[Is disclosed in column 6, lines 13-16 and column 8, lines 51-54]**

Blodgett discloses in column 6, lines 13-16, "The memory controller can include an address comparator which compares an address requested by the microprocessor and a new address generated by the memory controller."

Blodgett teaches a comparator configured to compare a signal corresponding to the request for data associated with a next read operation (new address generated by the memory controller) with a signal corresponding to the address for the read operation (address requested by the microprocessor). Blodgett further teaches that the memory controller is a buffer for the new address generated by itself.

With respect to **claim 13**,

"The memory controller of claim 11, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage is configured to issue a signal for distributing the data associated with the address and the data associated with the consecutive address in the temporary storage." **[is disclosed in column 3, lines 46-47, 66-67, column 4, lines 1-3, and FIG.3]**

Blodgett discloses in column 3, lines 66-67, column 4, lines 1-3 "For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the

first address specified by the row and column addresses is latched with the CAS* signal. Blodgett also discloses in column 3, lines 46-47, "The column address may be advanced with each CAS* transition, or each pulse."

Blodgett teaches a signal (CAS*) that is issued for distributing the data associated with the address (first address) and the data associated with the consecutive address (The column address may be advanced with each CAS* transition, or each pulse).

With respect to **claim 14**,

"The memory controller of claim 11, wherein the logic for requesting a read operation from memory originates from a microprocessor." **[is disclosed in column 1, lines 64-67 and column 2, lines 1-6]**

Blodgett discloses in column 1, lines 64-67 and column 2, lines 1-6, "...a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address. A memory controller is connected to the microprocessor and the synchronous memory device. The memory controller produces a second memory cell address and initiates a read operation in anticipation of a second data read operation at a new memory cell address provided from the microprocessor."

With respect to **claim 15**,

"The memory controller of claim 14, wherein the logic for storing both, data associated with the address and data associated with a consecutive address in

temporary storage includes, completing the storing prior to the microprocessor being capable of issuing any command following the read operation." **[is disclosed by Blodgett in column 1, lines 44-46 and lines 62-67]**

Blodgett discloses in column 1, lines 44-46 and lines 62-67, "a processor receiving data from a memory ay delay a new memory read operation until a prior read is complete...In particular, the present invention describes a system comprising a synchronous memory device having addressable memory cells, a microprocessor coupled to the synchronous memory device for data communication with the addressable memory cells, the microprocessor further initiating a data read operation at a first memory cell address."

Blodgett teaches completing the storing (data in memory) prior to the microprocessor being capable of issuing any command following the read operation (delay a new memory read operation until a prior read is complete).

With respect to **claim 19**,

"The integrated circuit of claim 16, wherein the core circuitry is configured as synchronous dynamic random access memory (SDRAM) circuitry." **[is disclosed by Blodgett in column 7, lines 31-32, and FIGs. 5 and 8]**

With respect to **claims 20 and 23**,

"The integrated circuit of claim 16, wherein the memory controller includes selection and storage logic configured to enable one of distribution of the data associated with the address and the consecutive address into the buffer, and access to the data associated with the address and the consecutive address

from the buffer, the access to the data being performed according to least significant bits of the second request." **[is disclosed in column 6, lines 53-61]**

The examiner interprets claim to mean that distribution for either the data address or the consecutive data address is enabled based on selection logic. The storage logic is implemented for access of the address and the consecutive address from the buffer. (Note: this limitation is interpreted as analogous to claim 11, and is therefore stated supra)

Blodgett discloses in column 6, lines 53-61, "...the present invention can include an address generator internal to the memory control circuitry 38 which produces a new column address if a valid new address is not provided on the external address lines. To assist the memory controller, the output enable (OE*) input can be used to indicate the presence of a valid address on the address lines. Further, additional counter circuitry can be added to the memory to enable the memory to output a full length column sequence."

Blodgett teaches the distribution for either the data address or the consecutive data address (both on address lines) is enabled based on selection logic (the output enable (OE*) input can be used to indicate the presence of a valid address on the address lines).

Claims 17 and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Blodgett in view of Laurenti in further view of Oberlaender et al. (US Patent No. 6,507,899 hereafter referred to as Oberlaender).

With respect to **claims 17 and 22**,

Blodgett teaches "The integrated circuit of claim 16..." as stated supra.

Blodgett, however, does not disclose expressly "...wherein the memory circuitry further comprises: a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and a second multiplexer configured to select the data associated with the consecutive

address when the second request is for the data associated with the second address."

Oberlaender discloses in column 1, lines 55-66, "The interface circuit comprises an address buffer having an input and an output, whereby the input receives an address signal from the data handling unit, a first multiplexer which couples the memory unit with either the output of the address buffer or with the address signal, a data buffer having an input and an output, the input receiving a data signal from the data handling unit and the output being coupled with the memory data input, a second multiplexer for selecting either the memory data signal output or the data buffer output, and a comparator for comparing the address signal with the signal from the address buffer output, generating a control signal which controls the second multiplexer."

Oberlaender further discloses in column 8, lines 15-28, "The next cycle is assumed to be a read cycle R3. During this cycle the now incoming data and control signals from the previous write cycle are buffered in registers 512 and 530. The previously stored address is copied from register 504 into register 503. The new incoming address is fed to the SRAM through multiplexer 500 which is switched to input 1 and stored in register 504. Comparator 505 compares the content of registers 504 and 503. In this case they are different. Therefore, multiplexer 520 is switched to input 0 and feeds the data read from the SRAM to the output D.sub.out '. Multiplexer 531 is switched to input 1 to couple the control signal WE' with the respective control input of the SRAM.

Blodgett and Oberlaender are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address, with the integrated circuit of claim 16 (or device of claim 21).

The motivation for doing so would have been obvious based on the teaching of Oberlaender in column 1, lines 5-42, "One of the main factors, which determine the speed of a microprocessor, is defined by the interface between the central processing unit and the memory...As in a reading instruction data will be

provided by the memory, only the memory access delay occurs and reading instructions can be executed in one cycle..."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Blodgett and Oberlaender before him/her to combine Oberlaender and Blodgett for the benefit of combine a first multiplexer configured to distribute the data associated with the address and the data associated with the consecutive address into the buffer; and a second multiplexer configured to select the data associated with the consecutive address when the second request is for the data associated with the second address, with the integrated circuit of claim 16 (or device of claim 21) to obtain the invention as specified in Claims 17 and 22.

Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Blodgett in view of Laurenti in further view of Le Pennec et al. (US Patent No. 6,920,488 hereafter referred to as Le Pennec).

With respect to **claims 25 and 26**,

Blodgett teaches "The device of claim 21..." as stated supra.

Blodgett, however, does not disclose expressly "...wherein the device is a portable handheld electronic device." or "...further comprising: a display screen configured to display image data."

Le Pennec discloses in column 4, lines 21-24, "The behavior of the PDA can be simulated on the portal server using a normal web browser. A web page

further can demonstrate the operability of the PDA screen and buttons." Le Pennec teaches a portable handheld electronic device (PDA or personal digital assistant) and also a display screen configured to display image data (PDA screen).

Blodgett and Le Pennec are analogous art because they are from the same field of endeavor, that being devices for processing data.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine a portable handheld electronic device (with a display screen configured to display image data) with the device of claim 21.

The motivation for doing so would have been obvious based on the teaching of Le Pennec in column 4, lines 11-15, "fields may be selected for viewing alone on the screen either by selecting the field by the pen of the PDA, or otherwise identifying the input field depending upon the capabilities of the PDA." Le Pennec also discloses in column 1, lines 12-14, "A Personal Digital Assistant which is a simple and small device fitting in the pocket, combines the portability..."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Blodgett and Le Pennec before him/her to combine Le Pennec and Blodgett for the benefit of having a portable handheld electronic device (with a display screen configured to display image data) with the device of claim 21 to obtain the invention as specified in Claims 25 and 26.

Response to Arguments

Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection. New grounds of rejection necessitated by applicant's amendments to the claims.

CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571)

272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

Supervisory Patent Examiner

Technology Center 2100